NAND Gate Based QCA 2-to-1 Line Multiplexer

Jin-Seong Lee, Jun-Cheol Jeon
Dept. of Computer Engineering, Kumoh National Institute of Technology
61, Daehak-ro, Gumi, Gyeongbuk 730-701, Korea
Leejinss01@gmail.com
1Corresponding Author : jcjeon@kumoh.ac.kr

Abstract. Quantum-dot cellular automata (QCA) is important technology to be replaced with CMOS. QCA is a new paradigm for digital computing that, theoretically, is expected to reach very high operating frequencies and significant reduction of power consumption. A multiplexer is an important element and it is used in many logic gates and functional circuits. A NAND gate is smaller, area-wise and faster than other circuits. In this paper we propose a new design of 2-to-1 line multiplexer using three NAND gates in QCA. We find an equation using De Morgan’s law and the equation can be presented by only AND and NOT logic. Thus we can implement a multiplexer by only NAND logics. Our structure reduced not only the number of cells but the required clock phases.

Keywords: Nanotechnology, Quantum-dot cellular automata, Majority gate, NAND gate, Multiplexer

1 Introduction

Quantum-dot cellular automata (QCA) is attracting a lot of attention due to its extremely small feature size (at the molecular and even atom level) and ultralow power consumption [1]. QCA offers a number of advantages over CMOS technology. Some of the advantages include faster switching speeds, high density circuits and far less power dissipation. The assumption is that all these advantages will result in the development of highly powerful and efficient computers [2, 3]. QCA devices encode and process binary information as charge configurations in arrays of coupled quantum dots, rather than current and voltage levels [4]. In the last few years, several basic QCA elements: a QCA cell, small binary wire, and digital logic gate, have been demonstrated [5]. However, in these devices the power gain needed for the operation of large QCA arrays was not achievable since the only source of energy was the signal input [4, 5].

A multiplexer is very important QCA circuits because they are expected to be used for addressing QCA random access memory arrays. The function of a Multiplexer is to select one input among a group of inputs and pass the selected input to output of the circuit. Basically it consists of two types of inputs: one group is the data input and the other group is the select input and these select inputs decide which data input is to be selected to pass to the output [5].

2 Related Work

2.1 QCA Basic

A quantum cell consists of four quantum dots located at the corners of a square and two extra electrons that can tunnel between the dots [6]. Normally two electrons are injected into the cell, where they occupy two dots on the two ends of one of the diagonals of the containing square cell [7]. Figure 1 shows a QCA cell and the Boolean nature of the polarization for its two electron configurations [8].
There are two primary QCA inverters which are a robust and simple one. Cells placed diagonally to each other have reverse polarizations. This characteristic is exploited to implement an inverter shown in Figure 2. Figure 2 (a) is a robust inverter and Figure 2 (b) is a simple inverter. A robust inverter is a stable state compared to simple inverter. A Simple inverter is better than robust inverter in number of cells. Another more important primary QCA gate realizes the 3-input majority function. This gate is composed of five QCA cells with a cross shape structure, as shown in Figure 2 (c) [7].

Figure 1. QCA cell: (a) Empty, (b) 1(Binary 1), (c) -1(Binary 0)

Figure 2. (a) A robust inverter, (b) Simple inverter, (c) QCA majority gates

2.2 Multiplexer

A multiplexer is a combinational circuit that selects binary information from one of many input lines and directs the information to a single output line. The selection of a particular input line is controlled by a set of input variables. A and B are the two inputs and S is used to select one between the two inputs. The functionality of multiplexer is shown in equation (1). A multiplexer is illustrated using three majority gates in Figure 3.

\[ F = AS' + BS \]  

(1)

Figure 3. Multiplexer diagram

3 Previous design

Many multiplexers have been proposed in various ways. Figure 4 has been proposed by other author [9]. The multiplexer use two majority AND gates, one majority OR gate and a robust inverter.
This structure consists of 37 cells and covers an area of 37,908nm². The multiplexer has many unnecessary cells so that it is not suitable for construction of a large circuit.

![Figure 4. Layout of proposed 2 to 1 multiplexer and simulation result [9]](image)

4 Proposed design

In this paper we propose 2-to-1 multiplexer in QCA. Our new design that we use equation using De Morgan’s law which is shown in equation (2). Our multiplexer diagram is proposed using three NAND majority gates shown in Figure 5. The NAND gates are implemented by three input majority gate with inverters. Our proposed 2-to-1 QCA multiplexer is shown in Figure 6. The design uses three majority AND gates and three inverters. We use two simple inverters to minimize the number of cell and one robust inverter to maximize a signal strength. We only use 31 cells over an area of 34,992nm². Our multiplexer has been designed using QCADesigner. Table 1 shows the truth table of proposed 2-to-1 multiplexer.

\[ F = (A + S')' + (B + S)' \]

![Figure 5. Proposed Multiplexer diagram](image)

Table 1. Truth table for proposed 2-to-1 multiplexer

<table>
<thead>
<tr>
<th>S</th>
<th>A</th>
<th>B</th>
<th>F</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>
5 Conclusions

Our design has focused on not only hardware complexity but also time complexity. As you see in Table 2, we have reduced the number of cells and area, and clock phases. We also have maximized area usage. In comparison, our design has 6.3% improvement in the area usage compared to previous structure. We have also used proper clock phases so that we have a strong signal with a compact structure. As a result, the proposed design is better than the previous structures.

<table>
<thead>
<tr>
<th>Table 2. Comparison of multiplexers</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hashemi et al. [9]</td>
</tr>
<tr>
<td>Number of cell</td>
</tr>
<tr>
<td>Total area (nm²)</td>
</tr>
<tr>
<td>Cell area (nm²)</td>
</tr>
<tr>
<td>Area usage (%)</td>
</tr>
<tr>
<td>Clock phase</td>
</tr>
</tbody>
</table>

References